



| | | | | | |
|---|--|---|---|---|---|
| II Year-II Semester | | L | T | P | C |
| | | 4 | 0 | 0 | 3 |
| SWITCHING THEORY AND LOGIC DESIGN (R1622023) | | | | | |

Course Outcomes:

Upon completion of the course, the student will be able to achieve the following outcomes.

| Cos | Course Outcomes | POs |
|-----|---|-----|
| 1 | To be able to understand review of number systems and binary codes | 4 |
| 2 | To be able to understand minimization techniques like boolean laws,k-map,tabular method | 4 |
| 3 | To be able to understand designing of combinational circuits | 4 |
| 4 | To be able to understand design of combinational circuits using PLDs | 4 |
| 5 | To be able to understand designing of sequential circuits-(FF,counters,Registers) | 4 |
| 6 | To be able to understand designing of FSM | 4 |

Syllabus:

UNIT I:

Objective: Understand the different number systems and different types of GATES and their operation and truth tables

REVIEW OF NUMBER OF SYSTEMS & CODES:

- i) Representation of numbers of different radix, conversion from one radix to another radix, r-1's compliments and r's compliments of signed members, problem solving.
- ii) 4 bit codes, BCD, Excess-3, 2421, 84-2-1 9's compliment code etc.,
- iii) Logic operations and error detection & correction codes; Basic logic operations -NOT, OR, AND, Universal building blocks, EX-OR, EX-NOR - Gates, Standard SOP and POS, Forms, Gray code, error detection, error correction codes (parity checking, even parity, odd parity, Hamming code) NAND-NAND and NOR-NOR realizations.

UNIT II:

Objective: Solve the given problem with the help of K-map, understand the duality and minimization techniques.

MINIMIZATION TECHNIQUES: Boolean theorems, principle of complementation & duality,De-morgan theorems, minimization of logic functions using Boolean theorems, minimization of switching functions using K-Map up to 6 variables, tabular minimization, problem solving (code-converters using K-Map etc..).



JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA
KAKINADA-533003, Andhra Pradesh, India
R-16 Syllabus for EEE.JNTUK

UNIT III:

Objective: Able to design the half adder, full adder and subtractors. Understand the different decoders and multiplexers.

COMBINATIONAL LOGIC CIRCUITS DESIGN:

Design of Half adder, full adder, half subtractor, full subtractor, applications of full adders, 4-bit binary subtractor, adder-subtractor circuit, BCD adder circuit, Excess 3 adder circuit, look-a-head adder circuit, Design of decoder, demultiplexer, 7 segment decoder, higher order demultiplexing, encoder, multiplexer, higher order multiplexing, realization of Boolean functions using decoders and multiplexers, priority encoder, 4-bit digital comparator.

UNIT IV:

Objective: Appreciate the ICs like PROM and understand the PLDs, PAL and PLA.

INTRODUCTION OF PLD's:

PROM, PAL, PLA-Basics structures, realization of Boolean function with PLDs, programming tables of PLDs, merits & demerits of PROM, PAL, PLA comparison, realization of Boolean functions using PROM, PAL, PLA, programming tables of PROM, PAL, PLA.

UNIT V:

Objective: Learn the functioning of different types of Flip-Flops, Registers and their operation and designing.

SEQUENTIAL CIRCUITS I:

Classification of sequential circuits (synchronous and asynchronous); basic flip-flops, truth tables and excitation tables (nand RS latch, nor RS latch, RS flip-flop, JK flip-flop, T flip-flop, D flip-flop with reset and clear terminals). Conversion from one flip-flop to flip-flop. Design of ripple counters, design of synchronous counters, Johnson counter, ring counter. Design of registers - Buffer register, control buffer register, shift register, bi-directional shift register, universal shift register.

UNIT VI:

Objective: Learn the finite state machine, Moore conversion and reduction of tables and realizing the circuits with flip flops.

SEQUENTIAL CIRCUITS II:

Finite state machine; Analysis of clocked sequential circuits, state diagrams, state tables, reduction of state tables and state assignment, design procedures. Realization of circuits using various flip-flops. Meelay to Moore conversion and vice-versa.

TEXT BOOKS:

1. Switching Theory and Logic Design by Hill and Peterson Mc-Graw Hill TMH edition.
2. Switching Theory and Logic Design by A. Anand Kumar.
3. Digital Design by Mano PHI.

REFERENCE BOOKS:

JAWAHARLAL NEHRU TECHNOLOGICAL UNIVERSITY: KAKINADA

KAKINADA-533003, Andhra Pradesh, India

R-16 Syllabus for EEE.JNTUK

1. Modern Digital Electronics by RP Jain, TMH.
2. Fundamentals of Logic Design by Charles H. Roth Jr, Jaico Publishers.
3. Microelectronics by Milliman MH edition.